REMARKS

This application has been carefully reviewed in light of the Office Action dated October 5, 2005. Claims 28 to 55 are in the application, of which Claims 50 to 55 have been newly added. Claims 28 to 33 and 39 to 44 have been amended and Claims 28, 33, 39, 44, 50 and 53 are the independent claims. Reconsideration and further examination are respectfully requested.

Claim 44 was objected to for an informality. Specifically, the claim was mistakenly labeled as "Currently Amended" when it was newly added. In this regard, the objection is believed to be moot, as Claim 44 is currently pending and amended in this Amendment and is therefore no longer newly added. Thus, Claim 44 is labeled as "Currently Amended". Withdrawal of this objection is therefore respectfully requested.

Claims 28 to 49 were rejected under 35 U.S.C. § 103(a) over U.S. Patent No. 6,128,747 (Thoulon) in view of the Applicants' Disclosed Background of the Invention ("ADBI"). Reconsideration and withdrawal of the rejections are respectfully requested.

Independent Claims 28 and 39

The invention of independent Claims 28 and 39 generally concerns power saving for a processor and a memory. Among its many features, the present invention includes the setting of a mode setting means to an enabled state in which the mode setting means is allowed to set the memory to a power saving mode.

Referring specifically to claim language, independent Claim 28 as amended is directed to an information processing apparatus. The apparatus includes processing means and mode setting means for setting a mode of a memory. The processing means sets the mode setting means to an enabled state in which the mode setting means is allowed to

set the memory to a power saving mode, and reads a power saving mode transfer instruction from the memory for setting the processing means to a power saving mode. The mode setting means sets the memory to the power saving mode while the mode setting means is in the enabled state, and the memory is set to the power saving mode in accordance with information which relates to the setting of the processing means to the power saving mode.

Independent Claim 39 as amended is directed to a power saving controlling method for a processor and a memory. The method includes an enabled state setting step of setting a memory controller for controlling the memory to an enabled state in which the memory controller is allowed to set the memory to a power saving mode. The method also includes a reading step of reading a power saving mode transfer instruction from the memory for setting the processor to a power saving mode. Additionally, the method includes a power saving mode setting step of setting the memory to a power saving mode while the memory controller is in the enabled state. The memory is set to the power saving mode in accordance with information which relates to the setting of the processor to the power saving mode.

In contrast, Applicants respectfully submit that the applied art, alone or in combination, is not seen to disclose or suggest at least the feature of setting a mode setting means to an enabled state in which the mode setting means is allowed to set the memory to a power saving mode.

As understood by Applicants, Thoulon discloses that an electronic device is provided with a processor which is responsive to the assertion of a sleep signal and which is able to emit a sleep acknowledgment signal and enter a low power mode. The device is also provided with a memory which is settable to a low power mode. Control of the

memory into its low power mode is effected by a sleep control circuit which sets the memory into its low power mode upon detection of the sleep acknowledgment signal emitted by the processor. See Thoulon, Abstract.

Page 3 of the Office Action asserts that Thoulon (Figure 1; Column 2, lines 18 to 24 and Column 3, line 65 to Column 4, line 8) discloses that a mode setting means "sets the memory into a power mode [sic, low power mode?] in accordance with a signal which relates to the setting of the processing means in the power saving mode and [is] inputted to said mode setting means while said mode setting means is in the enabled state."

However, even if Thoulon is seen to disclose a mode setting means, which is not conceded, Thoulon is still not seen to disclose or suggest at least the feature that the mode setting means is set, much less that it is set to an enabled state in which the mode setting means is allowed to set the memory to a power saving mode.

In particular, the portions of Thoulon cited by the Office Action disclose a processor which is responsive to the assertion of a sleep signal and which is able to emit a sleep acknowledgment signal and enter a low power mode, a memory settable in a low power mode, and sleep control means for setting the memory into its low power mode upon detection of the acknowledgment signal. See Thoulon, Column 2, lines 18 to 24. If the acknowledgment signal is sent on a bus, the means for detecting the acknowledgment signal and setting the memory into low power mode may be incorporated in the sleep control means in the memory controller. See Thoulon, Column 3, line 65 to Column 4, line 8.

Thus, Thoulon describes a simple signal exchange. In Thoulon, the processor receives the sleep signal and, prior to going to power save mode, issues an acknowledgment signal to the memory, which then goes to a power save mode. However,

this is not seen to disclose or suggest setting a mode setting means to an enabled state in which the mode setting means is allowed to set the memory in a power saving mode. Thoulon does not describe an enabled state at all, and thus cannot be read to disclose the setting of an enabled state. At best, it could be argued that Thoulon is in an "always enabled" state, but this still fails to disclose or suggest the setting of a mode setting means to an enabled state.

Therefore, for at least the foregoing reasons, Claims 28 and 39 are believed to be in condition for allowance and Applicants respectfully request same.

Independent Claims 33 and 44

The invention of independent Claims 33 and 44 generally concerns power saving for a processor and a memory. Among its many features, the invention of independent Claims 33 and 44 includes (i) setting a mode transfer means for transferring a mode of memory to a waiting state, and (ii) transferring the memory to a power saving mode after the end of the waiting state.

Referring specifically to claim language, independent Claim 33 is directed to an information processing apparatus. The apparatus includes processing means and mode transfer means for transferring a mode of a memory. The processing means sets the mode transfer means to a waiting state, and executes a power saving mode transfer instruction for setting the processing means to a power saving mode, and the mode transfer means transfers the memory to a power saving mode after the end of the waiting state.

Independent Claim 44 is directed to a power saving controlling method for a processor and a memory. The method includes a setting step of setting a memory controller for controlling the memory to a waiting state, an executing step of executing a power saving mode transfer instruction for setting the processor to a power saving mode,

and a transferring step of transferring the memory to a power saving mode after the end of the waiting state.

In contrast, Applicants respectfully submit that the applied art is not seen to suggest or disclose at least the features of (i) setting a mode transfer means for transferring a mode of memory to a waiting state and (ii) transferring the memory to a power saving mode after the end of the waiting state.

In particular, Applicants respectfully submit that the Office Action has failed to meet its burden under § 103(a). The Office Action concedes on page 4 that Thoulon does not disclose that the processing means sets the mode transfer means in a waiting state. In fact, Thoulon is not seen to disclose or suggest a memory controller capable of a waiting state. Specifically, Thoulon discloses that the processor responds to a sleep signal to enter a sleep or low power mode and the memory controller commands the memory to sleep, and this apparently occurs immediately upon recognition of the acknowledgment signal from the processor. See Thoulon, Column 3, lines 36 to 48 and Column 4, lines 4 to 8. In fact, Thoulon specifically states that "the [invention] provides for a quick setting of the memory into the sleep mode, as soon as the processor emits the sleep acknowledgment signal." Thoulon, Column 4, lines 35 to 38. The Office Action thus fails to show each and every feature of the claimed invention, specifically setting a memory controller in a waiting state, or a memory controller capable of a wait state.

Since there is no wait state, it naturally follows that there is no "end" to the wait state. As a consequence, it is impossible for the art to show a transfer of the memory to a power saving mode after the end of the wait state.

Therefore, for at least the foregoing reasons, Claims 33 and 44 are believed to be in condition for allowance and Applicants respectfully request same.

Independent Claims 50 and 53

New Claims 50 to 55 have been added and are directed to power saving for a processor and a memory. Among its many features, the invention of independent Claims 50 and 53 includes (i) setting the memory to the power saving mode in a case where a setting means is allowed to set the memory to the power saving mode, and (ii) detecting a signal relating to reading a power saving mode transfer instruction from the memory for setting the processor to a power saving mode.

Referring specifically to claim language, independent Claim 50 is directed to an information processing apparatus. The apparatus includes processing means, setting means for setting a mode of a memory, and detecting means for detecting a signal relating to reading a power saving mode transfer instruction from the memory for setting the processing means to a power saving mode. The signal is detected on a bus to which the processing means is connected. The setting means sets the memory to the power saving mode in a case where the setting means is allowed to set the memory to the power saving mode and where the signal is detected by the detecting means.

Independent Claim 53 is directed to a power saving controlling method for a processor and a memory. The method includes a detecting step of detecting a signal relating to reading a power saving mode transfer instruction from the memory for setting the processor to a power saving mode. The signal is detected on a bus to which the processor is connected. The method also includes an allowing step of allowing a memory controller to set the memory to a power saving mode. Additionally, the method includes a setting step of setting the memory to the power saving mode in a case where the memory controller is allowed in the allowing step to set the memory to the power saving mode and where the signal is detected in the detecting step.

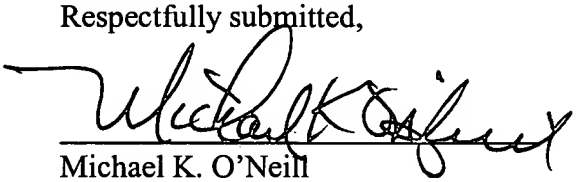
The art of record is not seen to disclose or suggest the features of Claims 50 and 53. Specifically, the art is not seen to suggest at least the features of (i) setting the memory to the power saving mode in a case where the setting means is allowed to set the memory to the power saving mode, and (ii) detecting a signal relating to reading a power saving mode transfer instruction from the memory for setting the processor to a power saving mode.

Thus, Claims 50 and 53 are believed to be in condition for allowance and Applicants respectfully request same.

The other claims in the application are each dependent from the independent claims discussed above and are therefore believed to be allowable over the applied references for at least the same reasons. Because each dependent claim is also deemed to define an additional aspect of the invention, however, the individual consideration of each on its own merits is respectfully requested.

Applicants' undersigned attorney may be reached in our Costa Mesa, California office at (714) 540-8700. All correspondence should continue to be directed to our below-listed address.

Respectfully submitted,



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